WHAT IS CLAIMED IS:

1. A method of plating an electrical contact on a substrate, comprising:

forming electrically connected plating layers on first and second opposing sides of a printed wiring board;

electroplating a contact layer over each of the plating layers using the plating layers; and

removing a portion of the plating layers from the first and second opposing sides while leaving the plating layers under the contact layer.

2. The method as recited in Claim 1 wherein forming electrically connected plating layers includes forming the electrically connected plating layers with an electro-less process and the method further includes electroplating a conductive layer on the plating layers.

3. The method as recited in Claim 1 wherein electroplating a contact layer includes electroplating a barrier layer over the plating layers.

4. The method as recited in Claim 3 wherein electroplating

a barrier layer includes electroplating a nickel layer and electroplating a contact layer further includes electroplating a gold layer on the nickel layer.

5. The method as recited in Claim 1 further including forming a discontinuous conductive layer on each of the plating layers and forming the plating layers includes forming a discontinuous plating layer on the first side.

6. The method as recited in Claim 1 wherein removing a portion of the plating layers includes removing a portion of the plating layer on the first side prior to electroplating the contact layer.

7. The method as recited in Claim 1 wherein removing a portion of the plating layers includes removing a portion of the plating layer on the second side subsequent to electroplating the contact layer.

8. A method of manufacturing an integrated circuit (IC) substrate, comprising:

forming a multi-layered substrate with a printed wiring board core and having metalized vias formed therethrough; and

plating an electrical contact on a surface of the substrate, including:

forming plating layers on first and second opposing sides of the substrate and on a via metal extending from the via to thereby electrically connect the plating layers;

electroplating a contact layer over each of the plating layers using the plating layers; and

removing a portion of the plating layers from the first and second opposing sides while leaving the plating layers under the contact layer.

9. The method as recited in Claim 8 wherein forming electrically connected plating layers includes forming the electrically connected plating layers with an electro-less process and the method further includes electroplating a conductive layer on the plating layers.

10. The method as recited in Claim 8 wherein electroplating a contact layer includes electroplating a barrier layer over the

plating layers.

11. The method as recited in Claim 10 wherein electroplating a barrier layer includes electroplating a nickel layer and electroplating a contact layer further includes electroplating a gold layer on the nickel layer.

12. The method as recited in Claim 8 further including forming a discontinuous conductive layer on each of the plating layers and forming the plating layers includes forming a discontinuous plating layer on the first side.

13. The method as recited in Claim 8 wherein removing a portion of the plating layers includes removing a portion of the plating layer on the first side prior to electroplating the contact layer.

14. The method as recited in Claim 8 wherein removing a portion of the plating layers includes removing a portion of the plating layer on the second side subsequent to electroplating the contact layer.

15. The method as recited in Claim 8 further including

forming openings in dielectric layers deposited on the first and second sides to contact the via metal and plating a contact includes plating the contact within the openings.

16. An integrated circuit (IC) substrate, comprising:

a dielectric layer located on opposing first and second sides of a printed wiring board and having openings formed therein;

a metalized via extending through the printed wiring board and having a via metal extending therefrom, the openings contacting the via metal;

a discontinuous plating layer located within each of the openings and contacting the via metal; and

an electroplated contact layer located over each of the discontinuous plating layers, the electroplated contact layers electrically connected to each other by the via metal.

17. The IC substrate as recited in Claim 16 further including an electroplated conductive layer located on each of the discontinuous plating layers.

18. The IC substrate as recited in Claim 16 wherein the electroplated contact layer includes a barrier layer located over each of the discontinuous plating layers.

19. The IC substrate as recited in Claim 18 wherein the barrier layer is an electroplated nickel layer and the contact layer further includes an electroplated gold layer located on the

electroplated nickel layer.

20. The IC substrate as recited in Claim 16 wherein each of the plating layers has a length that does not extend to an outer edge of the substrate such that the substrate is substantially free of a plating layer.